IN THE CLAIMS:

Please amend the claims as follows:

21. (Currently amended) An apparatus for detecting time-gap defects in a computer system having devices interconnected to one another, the apparatus comprising:

a memory device to store data structures comprising executables and operational data;

a processor operably connected to the memory device to process the data structures;

a controller to control an exchange of data between the devices; and

the memory device, wherein the data structures further comprise a detection module, executable by the processor and comprising:

an operation module to initiate an exchange of data producing a data stream between at least two of the devices,

a delay module to dynamically assign a value to a delay to be ~~imposed on the exchange~~ introduced into the data stream, and

a verification module to determine whether an error occurred ~~in the exchange,~~ as a result of the delay and remained undetected by the controller.

22. (Previously presented) The apparatus of claim 21, wherein the detection module is further programmed to receive an input for controlling the dynamic assignment of the value of the delay.

23. (Previously presented) The apparatus of claim 21, wherein the detection module is programmed to select the value iteratively.

24. (Previously presented) The apparatus of claim 23, wherein the detection module is programmed to iteratively select by a marching method over a time domain.

25. (Previously presented) The apparatus of claim 24, wherein the marching method comprises selecting an initial value and an increment, and stepping across at least a portion of the time domain by adding the increment to the value to select a new value.

26. (Previously presented) The apparatus of claim 23, wherein iteratively selecting comprises dynamically bracketing the value of the delay above which time gap errors occur and remain undetected by the controller.

27. (Previously presented) The apparatus of claim 21, wherein the detection module is programmed to dynamically bracket the value of the delay below which time gap errors do not occur and remain undetected by the controller.

28. (Previously presented) The apparatus of claim 21, wherein the detection module is programmed to iteratively select the value of the delay above which time gap errors occur.

29. (Previously presented) The apparatus of claim 21, wherein the detection module is programmed to iteratively select the value of the delay below which time gap errors do not occur.

30. (Currently amended) An article including a computer readable medium storing data structures comprising executables and operational data, the data structures comprising:

a control module to control an exchange of data between devices in a computer system, and to detect errors occurring in the exchange;

a detection module, executable to detect errors occurring due to a time gap and remaining undetected by the computer system, the detection module comprising:

an operation module to initiate an exchange of data producing a data stream between at least two of the devices;

a delay module to dynamically assign a value of a delay time to be ~~interposed in the exchange~~ introduced into the data stream; and

a verification module to determine whether an error occurred due to the delay time in the ~~exchange~~ data stream and remained undetected to the computer system.

31. (Previously presented) The article of claim 30, wherein the detection module is programmed to iteratively bracket a first value of the delay time, above which time gap errors occur and remain undetected by the control module, and a second value of the delay time, below which time gap errors do not occur and remain undetected by the control module.

32. (Currently amended) A method for detecting time-gap defects in components of a computer system, the method comprising:

providing a detection module to execute on a processor to initiate, detect, and verify reporting of errors that remain undetected to the computer system due to time gaps ~~in data exchanges~~ introduced into data streams communicated between devices in the computer system;

loading the detection module onto a computer system comprising a processor, a memory, devices connected to exchange data with one another, and controllers for controlling the exchange of data therebetween; and

executing the detection module by the processor to detect errors occurring and remaining otherwise undetected by the computer system due to the time gaps.

33. (Currently amended) The method of claim 32, wherein executing the detection module further comprises:

initiating an exchange of data producing a data stream between the devices in the computer system;

~~interposing~~ introducing a controlled delay in the ~~exchange~~ data stream;

checking the data for errors precipitated by the controlled delay ~~in the exchange~~; and

identifying devices incurring errors that remain undetected by the computer system.

34. (Currently amended) The method of claim 32, further comprising receiving operating parameters to ~~control a delay in the exchange~~ adjust the controlled delay to precipitate the errors.

35. (Currently amended) The method of claim 32, further comprising iteratively selecting

the value of ~~a delay in the exchange~~ the controlled delay.

36. (Currently amended) The method of claim 32, further comprising iteratively selecting the value of ~~a delay in the exchange~~ the controlled delay by a marching method over a time domain.